LINEAR HALF-RATE PHASE DETECTOR AND CLOCK AND DATA RECOVERY CIRCUIT

ABSTRACT OF THE DISCLOSURE

Method and apparatus for recovering a clock and data from a data signal. One method of the invention includes receiving the data signal having a first data rate, receiving the clock signal having a first clock frequency, alternating between a first level and a second level, wherein the first data rate is twice the first clock frequency. A first signal is generated by passing the data signal when the clock signal is at the first level, and storing the data signal when the clock signal is at the second level. A second signal is generated by passing the data signal when the clock signal is at the second level, and storing the data signal when the clock signal is at the first level. A third signal is generated by passing the first signal when the clock signal is at the second level, and storing the first signal when the clock signal is at the first level. A fourth signal is generated by passing the second signal when the clock signal is at the first level, and storing the second signal when the clock signal is at the second level. An error signal is generated by taking the exclusive-OR of the first signal and the second signal, and a reference signal is generated by taking the exclusive-OR of the third signal and the fourth signal.